# FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Replaces 512k x 8 volatile static RAM, EEPROM or Flash memory
- Unlimited write cycles
- Low-power CMOS
- Read and write access times as fast as 100ns
- Lithium energy source is electrically disconnected to retain freshness until power is applied for the first time
- Optional industrial temperature range of -40°C to +85°C, designated IND
- JEDEC standard 32-pin DIP package
- PowerCap Module (PCM) package
  – Directly surface-mountable module
  – Replaceable snap-on PowerCap provides lithium backup battery
  – Standardized pinout for all nonvolatile SRAM products
  – Detachment feature on PCM allows easy removal using a regular screwdriver

# PIN ASSIGNMENT
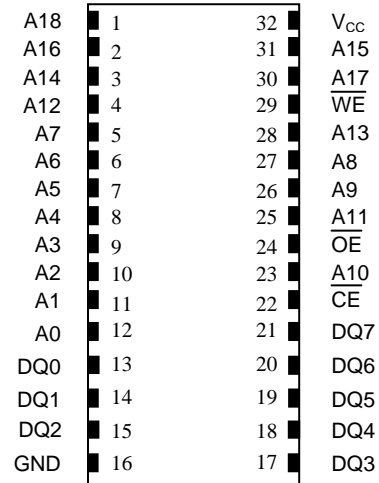


32-Pin Encapsulated Package
740-Mil Extended
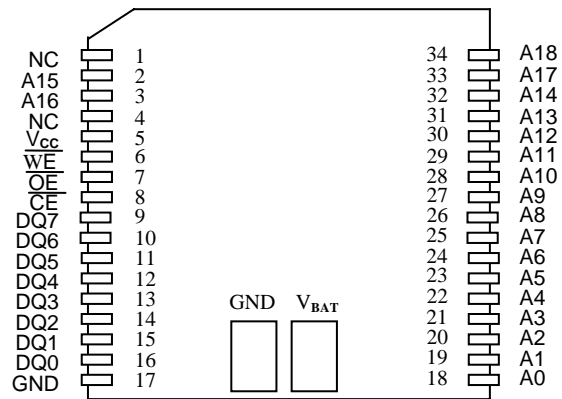


34-Pin PowerCap Module (PCM)
(Uses DS9034PC PowerCap)

# PIN DESCRIPTION

| | |
|---|---|
| A0 - A18 | - Address Inputs |
| DQ0 - DQ7 | - Data In/Data Out |
| $\overline{CE}$ | - Chip Enable |
| $\overline{WE}$ | - Write Enable |
| $\overline{OE}$ | - Output Enable |
| $V_{CC}$ | - Power (+3.3V) |
| GND | - Ground |
| NC | - No Connect |

# DESCRIPTION

The DS1250W 3.3V 4096k Nonvolatile SRAM is a 4,194,304-bit, fully static, nonvolatile SRAM organized as 524,288 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry, which constantly monitors $V_{CC}$ for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. DIP-package DS1250W devices can be used in place of existing 512k x 8 static RAMs directly conforming to the popular bytewide 32-pin DIP standard. DS1250W devices in the PowerCap Module package are directly surface mountable and are normally paired with a DS9034PC PowerCap to form a complete Nonvolatile SRAM module. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for microprocessor interfacing.

# READ MODE

The DS1250W executes a read cycle whenever $\overline{WE}$ (Write Enable) is inactive (high) and $\overline{CE}$ (Chip Enable) and $\overline{OE}$ (Output Enable) are active (low). The unique address specified by the 19 address inputs ($A_0$ - $A_{18}$) defines which of the 524,288 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within $t_{ACC}$ (Access Time) after the last address input signal is stable, providing that $\overline{CE}$ and $\overline{OE}$ (Output Enable) access times are also satisfied. If $\overline{OE}$ and $\overline{CE}$ access times are not satisfied, then data access must be measured from the later-occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either $t_{CO}$ for $\overline{CE}$ or $t_{OE}$ for $\overline{OE}$ rather than address access.

# WRITE MODE

The DS1250W executes a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are active (low) after address inputs are stable. The later-occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. $\overline{WE}$ must return to the high state for a minimum recovery time ($t_{WR}$) before another cycle can be initiated. The $\overline{OE}$ control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) then $\overline{WE}$ will disable the outputs in $t_{ODW}$ from its falling edge.

# DATA RETENTION MODE

The DS1250W provides full functional capability for $V_{CC}$ greater than 3.0 volts and write protects by 2.8 volts. Data is maintained in the absence of $V_{CC}$ without any additional support circuitry. The nonvolatile static RAMs constantly monitor $V_{CC}$. Should the supply voltage decay, the NV SRAMs automatically write protect themselves, all inputs become "don't care," and all outputs become high-impedance. As $V_{CC}$ falls below approximately 2.5 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when $V_{CC}$ rises above approximately 2.5 volts, the power switching circuit connects external $V_{CC}$ to RAM and disconnects the lithium energy source. Normal RAM operation can resume after $V_{CC}$ exceeds 3.0 volts.

# FRESHNESS SEAL

Each DS1250W device is shipped from Dallas Semiconductor with its lithium energy source disconnected, guaranteeing full energy capacity. When $V_{CC}$ is first applied at a level greater than 3.0 volts, the lithium energy source is enabled for battery back-up operation.

# PACKAGES

The DS1250W is available in two packages: 32-pin DIP and 34-pin PowerCap Module (PCM). The 32-pin DIP integrates a lithium battery, an SRAM memory and a nonvolatile control function into a single package with a JEDEC-standard 600-mil DIP pinout. The 34-pin PowerCap Module integrates SRAM

memory and nonvolatile control into a module base along with contacts for connection to the lithium battery in the DS9034PC PowerCap. The PowerCap Module package design allows a DS1250W PCM device to be surface mounted without subjecting its lithium backup battery to destructive high-temperature reflow soldering. After a DS1250W module base is reflow soldered, a DS9034PC PowerCap is snapped on top of the base to form a complete Nonvolatile SRAM module. The DS9034PC is keyed to prevent improper attachment. DS1250W module bases and DS9034PC PowerCaps are ordered separately and shipped in separate containers. See the DS9034PC data sheet for further information.

## ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground $\qquad$ -0.3V to +4.6V
Operating Temperature $\qquad$ 0°C to 70°C, -40°C to +85°C for IND parts
Storage Temperature $\qquad$ -40°C to +70°C, -40°C to +85°C for IND parts
Soldering Temperature

      DIP Module $\qquad$ +260°C for 10 seconds
      Caution: Do Not Reflow $\qquad$ (Wave or Hand Solder Only)
      PowerCap Module $\qquad$ See IPC/JEDEC J-STD-020

\*   This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS      ($t_A$: See Note 10)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 3.0 | 3.3 | 3.6 | V | |
| Logic 1 | $V_{IH}$ | 2.2 | | $V_{CC}$ | V | |
| Logic 0 | $V_{IL}$ | 0.0 | | +0.4 | V | |

## DC ELECTRICAL CHARACTERISTICS      ($t_A$: See Note 10) ($V_{CC}$=3.3V $\pm$ 0.3V)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Leakage Current | $I_{IL}$ | -1.0 | | +1.0 | μA | |
| I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$ | $I_{IO}$ | -1.0 | | +1.0 | μA | |
| Output Current @ 2.2V | $I_{OH}$ | -1.0 | | | mA | |
| Output Current @ 0.4V | $I_{OL}$ | 2.0 | | | mA | |
| Standby Current $\overline{CE}$ =2.2V | $I_{CCS1}$ | | 50 | 250 | μA | |
| Standby Current $\overline{CE}$ =$V_{CC}$-0.2V | $I_{CCS2}$ | | 30 | 150 | μA | |
| Operating Current | $I_{CCO1}$ | | | 50 | mA | |
| Write Protection Voltage | $V_{TP}$ | 2.8 | 2.9 | 3.0 | V | |

## CAPACITANCE      ($t_A$=25°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_{IN}$ | | 5 | 10 | pF | |
| Input/Output Capacitance | $C_{I/O}$ | | 5 | 10 | pF | |

## AC ELECTRICAL CHARACTERISTICS  (t$_A$: See Note 10) (V$_{CC}$=3.3V ± 0.3V)

| PARAMETER | SYMBOL | DS1250W-100 | | DS1250W-150 | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | | |
| Read Cycle Time | t$_{RC}$ | 100 | | 150 | | ns | |
| Access Time | t$_{ACC}$ | | 100 | | 150 | ns | |
| $\overline{OE}$ to Output Valid | t$_{OE}$ | | 50 | | 70 | ns | |
| $\overline{CE}$ to Output Valid | t$_{CO}$ | | 100 | | 150 | ns | |
| $\overline{OE}$ or $\overline{CE}$ to Output Active | t$_{COE}$ | 5 | | 5 | | ns | 5 |
| Output High Z from Deselection | t$_{OD}$ | | 35 | | 35 | ns | 5 |
| Output Hold from Address Change | t$_{OH}$ | 5 | | 5 | | ns | |
| Write Cycle Time | t$_{WC}$ | 100 | | 150 | | ns | |
| Write Pulse Width | t$_{WP}$ | 75 | | 100 | | ns | 3 |
| Address Setup Time | t$_{AW}$ | 0 | | 0 | | ns | |
| Write Recovery Time | t$_{WR1}$ | 5 | | 5 | | ns | 12 |
| | t$_{WR2}$ | 20 | | 20 | | | 13 |
| Output High Z from $\overline{WE}$ | t$_{ODW}$ | | 35 | | 35 | ns | 5 |
| Output Active from $\overline{WE}$ | t$_{OEW}$ | 5 | | 5 | | ns | 5 |
| Data Setup Time | t$_{DS}$ | 40 | | 60 | | ns | 4 |
| Data Hold Time | t$_{DH1}$ | 0 | | 0 | | ns | 12 |
| | t$_{DH2}$ | 20 | | 20 | | | 13 |

## READ CYCLE



SEE NOTE 1

# WRITE CYCLE 1



SEE NOTES 2, 3, 4, 6, 7, 8, AND 12
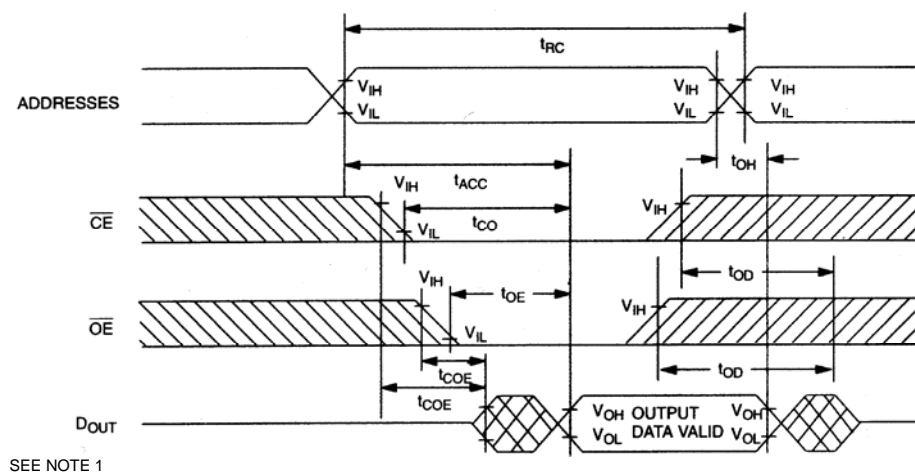
# WRITE CYCLE 2
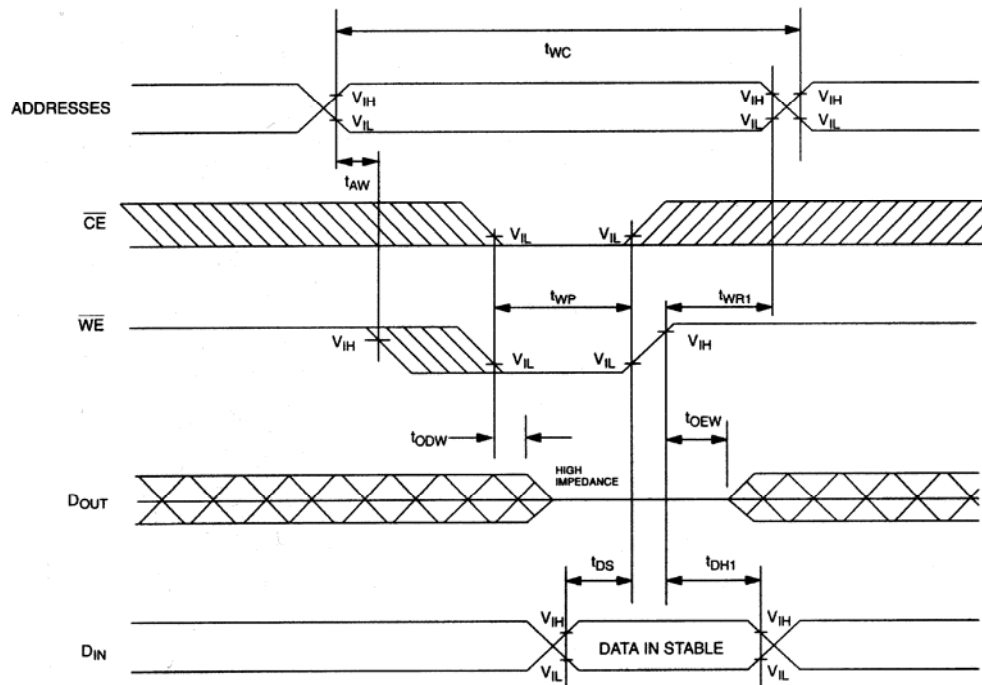


SEE NOTES 2, 3, 4, 6, 7, 8, AND 12
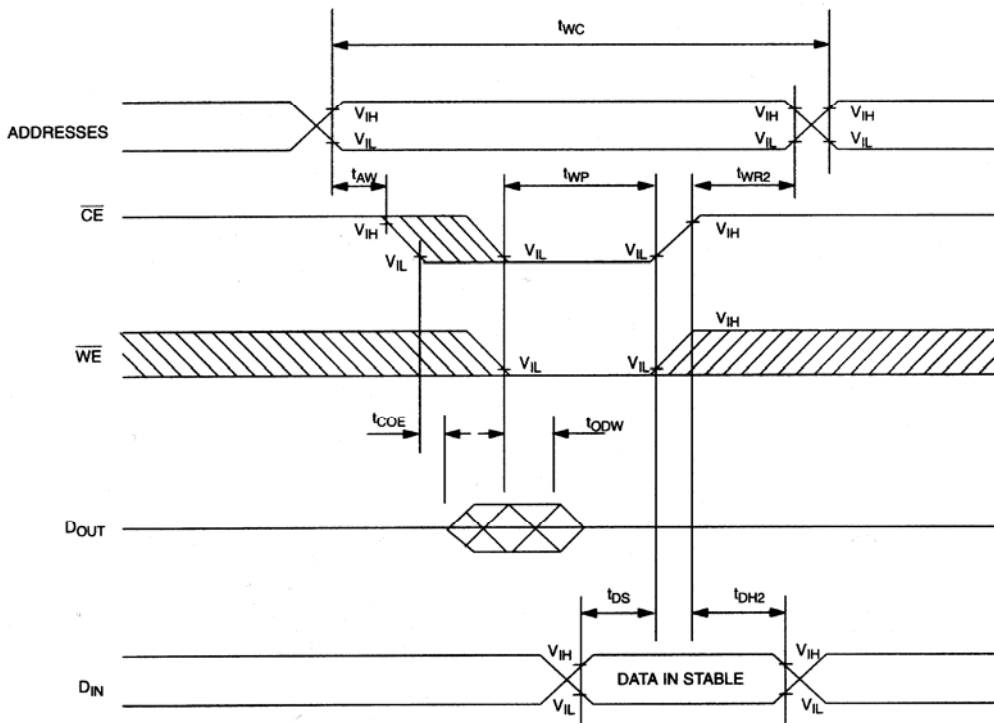
## POWER-DOWN/POWER-UP CONDITION
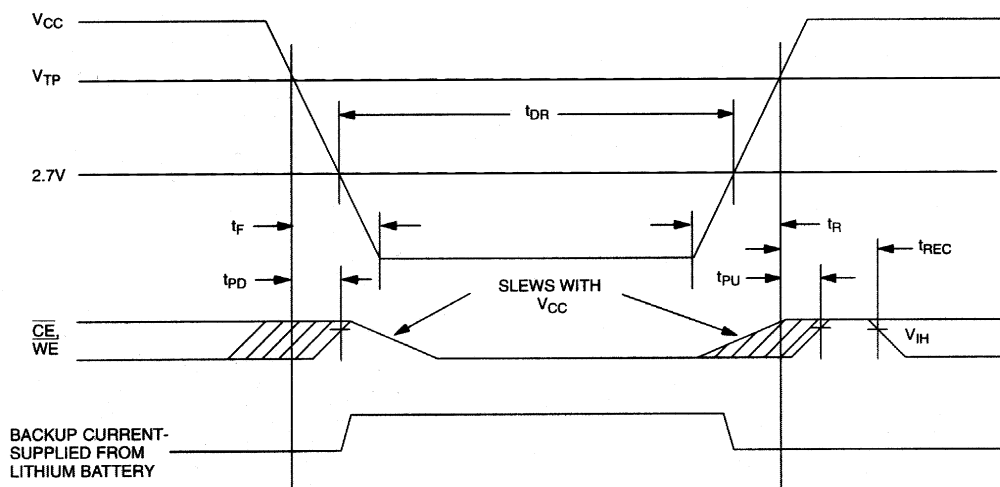


## POWER-DOWN/POWER-UP TIMING                    (t$_A$: See Note 10)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| V$_{CC}$ Fail Detect to $\overline{CE}$ and $\overline{WE}$ Inactive | t$_{PD}$ | | | 1.5 | μs | 11 |
| V$_{CC}$ slew from V$_{TP}$ to 0V | t$_F$ | 150 | | | μs | |
| V$_{CC}$ slew from 0V to V$_{TP}$ | t$_R$ | 150 | | | μs | |
| V$_{CC}$ Valid to $\overline{CE}$ and $\overline{WE}$ Inactive | t$_{PU}$ | | | 2 | ms | |
| V$_{CC}$ Valid to End of Write Protection | t$_{REC}$ | | | 125 | ms | |

(t$_A$=25°C)

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Expected Data Retention Time | t$_{DR}$ | 10 | | | years | 9 |

## WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

## NOTES:

1. $\overline{WE}$ is high for a Read Cycle.
2. $\overline{OE}$ = V$_{IH}$ or V$_{IL}$. If $\overline{OE}$ = V$_{IH}$ during write cycle, the output buffers remain in a high-impedance state.
3. t$_{WP}$ is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t$_{WP}$ is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t$_{DH}$, t$_{DS}$ are measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
5. These parameters are sampled with a 5 pF load and are not 100% tested.
6. If the $\overline{CE}$ low transition occurs simultaneously with or latter than the $\overline{WE}$ low transition, the output buffers remain in a high-impedance state during this period.
7. If the $\overline{CE}$ high transition occurs prior to or simultaneously with the $\overline{WE}$ high transition, the output buffers remain in high-impedance state during this period.

8. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high-impedance state during this period.

9. Each DS1250W has a built-in switch that disconnects the lithium source until $V_{CC}$ is first applied by the user. The expected $t_{DR}$ is defined as accumulative time in the absence of $V_{CC}$ starting from the time power is first applied by the user.

10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is -40°C to +85°C.

11. In a power-down condition the voltage on any pin may not exceed the voltage on $V_{CC}$.

12. $t_{WR1}$ and $t_{DH1}$ are measured from $\overline{WE}$ going high.

13. $t_{WR2}$ and $t_{DH2}$ are measured from $\overline{CE}$ going high.

14. DS1250 modules are recognized by Underwriters Laboratory (U.L.®) under file E99151.

## DC TEST CONDITIONS
Outputs Open
Cycle = 200ns for operating current
All voltages are referenced to ground

## AC TEST CONDITIONS
Output Load: 100 pF + 1TTL Gate
Input Pulse Levels: 0 to 2.7V
Timing Measurement Reference Levels
     Input:  1.5V
     Output:  1.5V
Input pulse Rise and Fall Times:  5ns

## ORDERING INFORMATION

| Part Number | Temperature Range | Supply Tolerance | Pin/Package | Speed Grade |
|---|---|---|---|---|
| DS1250W-100 | 0°C to +70°C | 3.3V ± 0.3V | 32 / 740 EMOD | 100ns |
| DS1250W-100+ | 0°C to +70°C | 3.3V ± 0.3V | 32 / 740 EMOD | 100ns |
| DS1250WP-100 | 0°C to +70°C | 3.3V ± 0.3V | 34 / PowerCap* | 100ns |
| DS1250WP-100+ | 0°C to +70°C | 3.3V ± 0.3V | 34 / PowerCap* | 100ns |
| DS1250W-100IND | -40°C to +85°C | 3.3V ± 0.3V | 32 / 740 EMOD | 100ns |
| DS1250W-100IND+ | -40°C to +85°C | 3.3V ± 0.3V | 32 / 740 EMOD | 100ns |
| DS1250WP-100IND | -40°C to +85°C | 3.3V ± 0.3V | 34 / PowerCap* | 100ns |
| DS1250WP-100IND+ | -40°C to +85°C | 3.3V ± 0.3V | 34 / PowerCap* | 100ns |
| DS1250W-150 | 0°C to +70°C | 3.3V ± 0.3V | 32 / 740 EMOD | 150ns |
| DS1250W-150+ | 0°C to +70°C | 3.3V ± 0.3V | 32 / 740 EMOD | 150ns |
| DS1250WP-150 | 0°C to +70°C | 3.3V ± 0.3V | 34 / PowerCap* | 150ns |
| DS1250WP-150+ | 0°C to +70°C | 3.3V ± 0.3V | 34 / PowerCap* | 150ns |

*+ Denotes lead-free/RoHS-compliant product.*
*\* DS9034PC or DS9034PCI (PowerCap) required. Must be ordered separately.*

## PACKAGE INFORMATION
(For the latest package outline information, go to **http://www.maxim-ic.com/DallasPackInfo**.)

| PACKAGE TYPE | DOCUMENT NO. |
|---|---|
| 32 DIP | **56-G0002-001** |

# DS1250W NONVOLATILE SRAM, 34-PIN POWERCAP MODULE
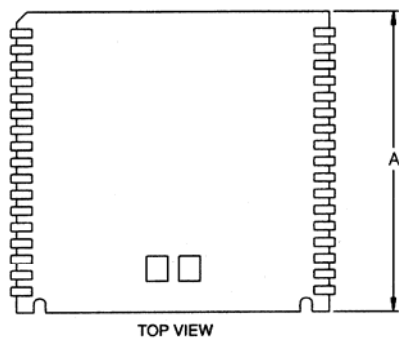
| PKG DIM | INCHES | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.920 | 0.925 | 0.930 |
| B | 0.980 | 0.985 | 0.990 |
| C | - | - | 0.080 |
| D | 0.052 | 0.055 | 0.058 |
| E | 0.048 | 0.050 | 0.052 |
| F | 0.015 | 0.020 | 0.025 |
| G | 0.020 | 0.025 | 0.030 |

TOP VIEW

SIDE VIEW

.004

BOTTOM VIEW: REFERENCE ONLY
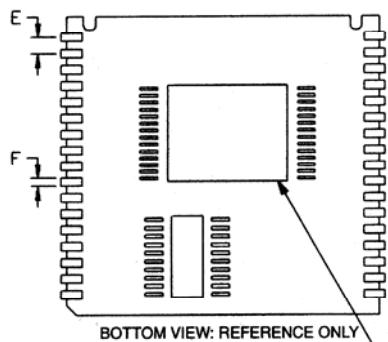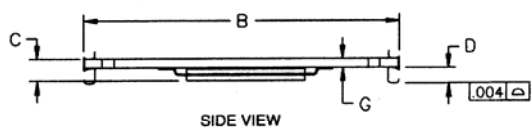
COMPONENTS AND PLACEMENTS
MAY DIFFER FROM THOSE SHOWN

## DS1250W NONVOLATILE SRAM, 34-PIN POWERCAP MODULE WITH POWERCAP



TOP VIEW

SIDE VIEW

BOTTOM VIEW: REFERENCE ONLY

COMPONENTS AND PLACEMENTS
MAY DIFFER FROM THOSE SHOWN
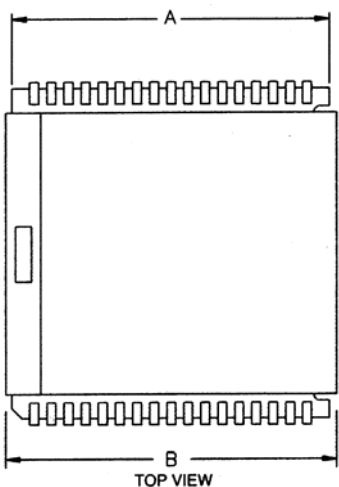
| PKG DIM | INCHES | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.920 | 0.925 | 0.930 |
| B | 0.955 | 0.960 | 0.965 |
| C | 0.240 | 0.245 | 0.250 |
| D | 0.052 | 0.055 | 0.058 |
| E | 0.048 | 0.050 | 0.052 |
| F | 0.015 | 0.020 | 0.025 |
| G | 0.020 | 0.025 | 0.030 |
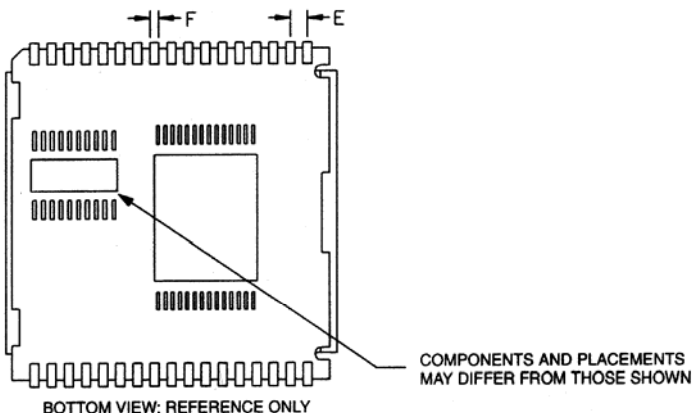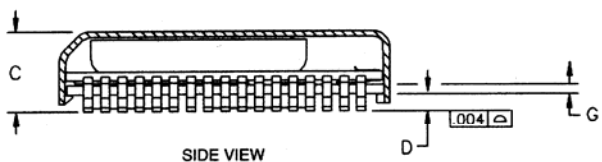
## ASSEMBLY AND USE

Reflow soldering
Dallas Semiconductor recommends that PowerCap Module bases experience one pass through solder reflow oriented label-side up (live-bug).

Hand soldering and touch-up
Do not touch soldering iron to leads for more than 3 seconds. To solder, apply flux to the pad, heat the lead frame pad and apply solder. To remove part, apply flux, heat pad until solder reflows, and use a solder wick.

LPM replacement in a socket
To replace a Low Profile Module in a 68-pin PLCC socket, attach a DS9034PC PowerCap to a module base then insert the complete module into the socket one row of leads at a time, pushing only on the corners of the cap. Never apply force to the center of the device. To remove from a socket, use a PLCC
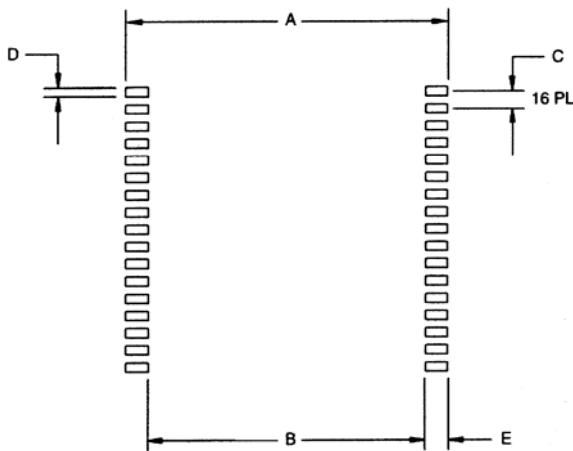
extraction tool and ensure that it does not hit or damage any of the module IC components. Do not use any other tool for extraction.

## RECOMMENDED POWERCAP MODULE LAND PATTERN
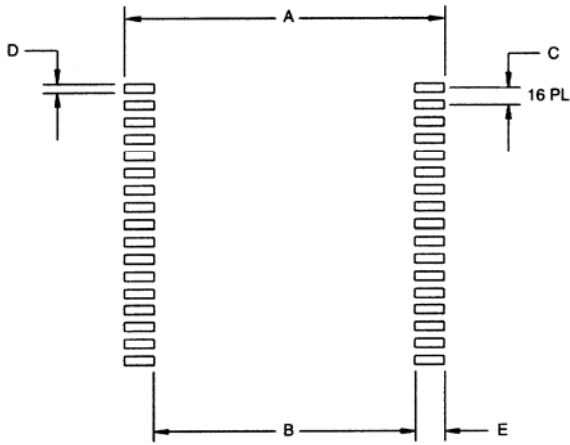


| PKG DIM | INCHES | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | 1.050 | - |
| B | - | 0.826 | - |
| C | - | 0.050 | - |
| D | - | 0.030 | - |
| E | - | 0.112 | - |

## RECOMMENDED POWERCAP MODULE SOLDER STENCIL



| PKG DIM | INCHES | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | - | 1.050 | - |
| B | - | 0.890 | - |
| C | - | 0.050 | - |
| D | - | 0.030 | - |
| E | - | 0.080 | - |

# REVISION HISTORY

| REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|
| 121907 | Added package information table.<br><br>Removed the DIP module package drawing and dimension table. | 7, 8 |